REMARKS

Claims 1-4, 8-9, and 13-19 were previously pending. Claims 1-2 have been amended. Claims 8-9 have been cancelled. Claims 20-21 are new. Thus, after entry of this amendment, claims 1-4 and 13-21 are currently pending. No new matter has been added.

Advisory Action

In the Advisory Action dated January 25, 2011, the Examiner suggested clarifying the subject matter of the present claims to eliminate a broader interpretation thereof.

In response, the present claims have been amended to distinctly claim the subject matter of the present application.

Claims Rejections - 35 U.S.C. § 103

In the Final Office Action dated October 19, 2010, claims 1-4, 8-9, and 13-19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Stallkamp (US 6,895,009) in view of Domon (US 2003/0014679).

Applicant respectfully traverses these rejections. Applicant respectfully asserts that the cited references, alone or in any combination, fail to disclose, teach, or even suggest each and every limitation of the present claims.

For instance, Stallkamp does not disclose or even suggest a data conversion unit, in a manner as recited in the present claims. In fact, as conceded by the Action in pg. 3, Stallkamp fails to disclose or even suggest transmitting first image data (e.g., a video signal in DV format) and converting the first image data to second image data (e.g., an analog video signal or a video signal in SDI format), in a manner as recited in the present claims.

Instead, Stallkamp merely discloses synchronizing frequency of timing signals and, as such, does not disclose, teach, or even suggest the production or conversion of data signals, in a manner as recited in the present claims.

Moreover, Domon fails to remedy the deficiencies of Stallkamp. For instance, Domon is merely relied on for teaching a digital video player 220 in Fig. 11 that decodes a digital video signal and outputs an analog video signal. However, there appears to be no apparent reason why one of ordinary skill in the art at the time when the invention was made would have combined the disclosures of the cited references to read on the present claims. The present application, in

- 6 -

one aspect, refers to synchronizing data transfer with converted data output (*see Abstract*). In contrast to the present claims, Domon is merely directed to updating slave nodes timing parameters with a master timing signal. Even though Domon teaches a digital video player 220, Domon fails to disclose or even suggest a first node configured to transmit first image data to a second node at a transfer rate synchronized with a cycle start packet output from the cycle master and the second node having a data conversion unit configured to synchronize second image data generated by conversion of the first image data in the second node with an external reference signal, in a manner as recited in the present claims.

In contrast to the Stallkamp and Domon references, present independent claim 1 recites the following limitations (***emphasis added***):

> a first node and a second node in which one of the first node and the second node on an IEEE1394 bus serves as a cycle master, ***the first node being configured to transmit <u>first image data</u> to the second node at a transfer rate synchronized with a cycle start packet output from the cycle master, <u>the second node having a data conversion unit configured to synchronize second image data generated by conversion of the first image data in the second node with an external reference signal, the second node to output the second image data,</u>***
> an external synchronizing signal receiver for receiving the external reference signal provided on at least one of the first and second nodes, and
> a synchronization adjustment unit for synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal.

Applicant respectfully submits that Stallkamp fails to disclose, teach, or even suggest, "the second node having a data conversion unit configured to synchronize second image data generated by conversion of the first image data in the second node with an external reference signal, the second node to output the second image data," as recited in present claim 1.

Instead, in col. 5, lines 63-67, Stallkamp merely discloses a synchronizer 254 having a frame rate converter 304 that <u>samples</u> audio and video signals at a nominal rate based on a local clock output signal 309. In fact, Stallkamp explicitly discloses that frame rate converter 304 <u>operates as a frequency sampler</u> for sampling the frequency of local clock output signal 309. Clearly, frame rate converter 304 is merely a frequency sampler and <u>not</u> a data conversion unit for converting data, in a manner as recited in present claim 1. Clearly, Stallkamp fails to disclose or even suggest a second node having a data conversion unit configured to synchronize second

- 7 -

image data generated by conversion of the first image data in the second node with an external reference signal and the second node to output the second image data, in a manner as recited in present claim 1.

Further, in reference to col. 5, lines 31-40, Stallkamp discloses that synchronizer 254 includes a local clock 302 for producing a series of clock pulses and providing timing signals. In col. 5, lines 58-67, frame rate converter 304 generates a desired synchronous output signal 310 *measured in frames per second* based on a substantially fixed input frequency of clock output 309 from local clock 302. As such, Stallkamp is only concerned with synchronizing frequency of timing signals, and Stallkamp only produces timing singles and not data signals.

Since Stallkamp is not concerned with converting data (e.g., video image data) from one data format (e.g., video signal in DV format) to another data format (e.g., analog video signal or video signal in SDI format), Stallkamp fails to disclose or even suggest a data conversion unit, in a manner as recited in present claim 1. To the extent that Stallkamp discloses synchronizer 254 having frame rate converter 304 that synchronizes frequency of synchronizer clock 310 to local clock 309, Stallkamp fails to disclose or even suggest that synchronizer 254 is a second node having a data conversion unit configured to synchronize second image data generated by conversion of the first image data in the second node with an external reference signal, in a manner as recited in present claim 1.

Moreover, Applicant respectfully submits that Stallkamp fails to disclose, teach, or even suggest, "the second node to output the second image data," in a manner as recited in present claim 1. In reference to previous remarks, since Stallkamp does not disclose or even suggest a data converting unit, Stallkamp does not disclose or even suggest converting first image data to second image data and outputting the second image data from the second node, in a manner as recited in present claim 1. In fact, the Action fails to properly address this claimed limitation. In the last line of pg. 2, it appears that the Action concedes that Stallkamp does not disclose or suggest this limitation by asserting that Stallkamp discloses, "the second node not to output the data." Clearly, the Action raises uncertainty in this regard. As such, Applicant respectfully requests clarification in regard to this assertion by the Action.

As conceded by the Action in pg. 3, Applicant respectfully submits that Stallkamp fails to disclose, teach, or even suggest, "the first node being configured to transmit first image data to the second node at a transfer rate synchronized with a cycle start packet output from the cycle

- 8 -

master," in a manner as recited in present claim 1. The Action purports that Domon discloses this subject matter. However, Applicant respectfully asserts that Domon fails to remedy the deficiencies of Stallkamp. For instance, Domon is merely relied on for purportedly teaching a digital video player 220 in Fig. 11 that decodes a digital video signal and outputs an analog video signal. There appears to be no apparent reason why one of ordinary skill in the art at the time when the invention was made would have combined the disclosures of the cited references to read on present claim 1. The present application, in one aspect, refers to synchronizing data transfer with converted data output (*see Abstract*). In contrast, Domon is merely directed to updating slave nodes timing parameters with a master timing signal. Clearly, Domon fails to disclose or even suggest a first node configured to transmit first image data to a second node at a transfer rate synchronized with a cycle start packet output from the cycle master, the second node having a data conversion unit configured to synchronize second image data generated by conversion of the first image data in the second node with an external reference signal, the second node to output the second image data, in a manner as recited in the present claims.

Applicant respectfully submits that the Stallkamp reference fails to disclose, teach, or suggest each and every limitation of present claim 1, and since the ancillary Domon reference fails to remedy the deficiencies of Stallkamp, present independent claim 1 including any claims dependent thereon are considered to be in condition for allowance, and such allowance is respectively requested.

Claims 2-4 and 13-19 are dependent on independent claim 1 and therefore include all of limitations of independent claim 1 and additional limitations therein. As such, these claims are considered to be in condition for allowance for at least their respective dependence on claim 1.

Present independent claims 20-21 are new and are considered to be in condition for allowance for at least the same reasons as discussed above in reference to present independent claim 1, and such allowance is respectively requested.

For at least the reasons discussed herein, present claims 1-4 and 13-21 are not anticipated or considered obvious over the cited references, alone or in any combination. Therefore, reconsideration of present claims 1-4 and 13-21 is respectfully requested with express withdrawal of the rejections under 35 U.S.C. § 103(a).

LA/386231.2

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-4 and 13-21 in the application are patentable. Accordingly, reconsideration and allowance of this application are earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

In the event that any fees are due with respect to this paper, please charge Deposit Account No. 01-2300, referencing Atty. Docket No. 033163-00762.

Respectfully submitted,

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- 10 -